multiplexing means is connected and configured to provide row addresses, column addresses and data on the bus." and substitute:--Instruction fetching means are connected to the bus to fetch instruction groups via the bus from the memory. Each of the instruction groups include at least one instruction that accesses operands or instructions or both. The operands and instructions are located relative to the instruction groups. An instruction register receives a first of the instruction groups from the instruction fetching means. The first of the instruction groups include one or more sequential instructions. Instruction supplying means supplies, in succession from the instruction register, the one or more sequential instructions of the first of the instruction groups to the central processing unit. An instruction decoding means configures the instruction supplying means to select from the instruction register an operand associated with one of the instructions from the first of the instruction groups.--.

Page 3, lines 15-25, delete "system has a means connected to the bus for fetching instructions for the central processing unit on the bus. The means for fetching instructions is configured to fetch multiple sequential instructions in a single memory cycle. In a variation of this aspect of the invention, a programmable read only memory containing instructions for the central processing unit is connected to the bus. The means for fetching instructions includes means for assembling a plurality of instructions from the programmable read only memory and storing the plurality of instructions in the dynamic random access memory." and substitute --has a central processing unit and an instruction register operatively coupled to the central processing unit. An instruction fetching means provides instruction groups to the instruction register wherein certain of the instruction groups include one or more operands or sequential instructions or both. The one or more sequential instructions including at least one instruction that accesses operands or instructions or both being located relative to the instruction groups. An instruction supplying means successively couples the one or more sequential instructions of the certain of the instruction groups to the central processing unit. An instruction decoding means configures the instruction supplying means to select operands from the instruction register associated with particular ones of the sequential instructions.--.

Page 3, lines 28-32, delete "a direct memory access processing unit and a memory connected by a bus. The direct memory access processing unit includes